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ART-UNIT: 215
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ABSTRACT:
The communications processor of the present invention comprises, in a single integrated circuit chip, the combination of a central processing unit (CPU) having an execution unit with an arithmetic logic unit and accumulators, a program counter, memory, a clock generator, a timer, a bus

interface, chip
select outputs, and an interrupt **processor; a digital signal processor (DSP)**
having an instruction set to carry out a **digital signal processing** algorithm,
an execution unit for carrying out multiply and accumulate operations and an
external interface; an address bus connected between the CPU and the **DSP**; a
data bus connected between the CPU and the **DSP**; and a static scheduler for
statically scheduling execution of the signal processing algorithm between the
**digital signal processor** and the CPU.

15 Claims, 23 Drawing figures

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APD:
**19900706**

TTL:
Communications **processor for voice** band telecommunications

ABPL:
The communications processor of the present invention comprises, in a single
integrated circuit chip, the combination of a central processing unit (CPU)
having an execution unit with an arithmetic logic unit and accumulators, a
program counter, memory, a clock generator, a timer, a bus interface, chip
select outputs, and an interrupt **processor; a digital signal processor (DSP)**
having an instruction set to carry out a **digital signal processing** algorithm,
an execution unit for carrying out multiply and accumulate operations and an
external interface; an address bus connected between the CPU and the **DSP**; a
data bus connected between the CPU and the **DSP**; and a static scheduler for
statically scheduling execution of the signal processing algorithm between the

digital signal processor and the CPU.

BSPR:
This invention relates to processors for voice band telecommunications and more particularly to digital processors which have the capability of processing code excited linear predictive algorithms.

BSPR:
Currently, digital signal processors (DSPs) such as the DSP65000 family manufactured by Motorola, Inc. are available for implementing digital algorithms such as digital filters, fast fourier transforms, correlation functions, etc. Such processors have special features such as modulo addressing, hardware DO loops, 24-bit by 24-bit hardware multipliers, etc. to facilitate the large number of high precision arithmetic operations required in digital signal processing. DSPs are ideally suited for executing the VSELP and similar algorithms except that current models have too low a clock rate. The DSP65000 family, for example has a nominal clock rate of 20.48 MHz giving an execution rate of 10.24 MIPS. This can be increased to 27 MHz for an execution rate of 13.5 MIPS. To accomodate the 15.6 MIPS needed for IS-54, the clock rate would have to be increase to about 32 MHz. Such an increase would require redesign of the DSP.

BSPR:
One object of the present invention is to provide a communications processor for implementing IS-54 and other computationally intensive digital signal processing algorithms using conventionally available components operating at conventional clock rates.

BSPR:
Another object of the present invention is to provide a

communications
processor which contains a user programmable functionality permitting the
execution of instructions in addition to the computationally intensive **digital signal processing** algorithm without adversely affecting execution of the
algorithm.

BSPR:
In accordance with the above and other objects, the communications processor of
the present invention comprises, in a single integrated circuit chip, the
combination of a central processing unit (CPU) having an execution unit with an
arithmetic logic unit and accumulators, a program counter, memory, a clock
generator, a timer, a bus interface, chip select outputs, and an interrupt
**processor; a digital signal processor (DSP)** having an instruction set to carry
out a **digital signal processing** algorithm, an execution unit for carrying out
multiply and accumulate operations and an external interface; an address bus
connected between the CPU and the **DSP**; a data bus connected between the CPU and
the **DSP**; and a static scheduler for statically scheduling execution of the
signal processing algorithm between the **digital signal processor** and the CPU.

BSPR:
In accordance with other aspects, the **digital signal processing** algorithm may
be a digital speech processing algorthim and the scheduler may be contained in
the **DSP** and may include an interrupt generator for generating interrupts to the
CPU to command execution by the CPU of portions of the speech processing
algorithm. The CPU interrupt processor processes the interrupts from the **DSP**
as nonmaskable interrupt signals to ensure that execution of the algorithm
takes priority over other programs.

BSPR:
To exploit the advantages of the **DSP** and CPU, the static scheduler partitions
execution of the signal processing algorithm to cause all multiply and
multiply-accumulate operations to be executed in the **DSP** and all other
operations such as add, subtract, divide, compare, etc. to be executed in the
CPU.

BSPR:
The static scheduler effects simultaneous operation of the CPU and **DSP** during
portions of the execution of said signal processing algorithm.

DRPR:
FIG. 1 is a block diagram showing the **main components of the communications
processor** of the present invention;

DRPR:
FIG. 12 is a functional block diagram showing the **digital transmit signal flow
of the processor** configured as in FIG. 10;

DRPR:
FIG. 13 is a functional block diagram showing the **digital receive signal flow
of the processor** configured as in FIG. 10;

DRPR:
FIG. 19 is timing diagram useful with table 1 to show the partitioning of
arithmetic operations between the **digital signal processor** and the central
processing unit of FIG. 2 when implementing a VSELP algorithm;

DEPR:
One of the key elements of the architecture is the unique combination of a
standard microprocessor shown in FIG. 1 as CPU 200 with a dedicated custom **DSP**
engine shown in FIG. 1 as multiplier-accumulator (MAC)

engine 300 and a
multi-port static RAM (SRAM) 400 to process the VSELP and GSM speech
compression algorithms. This combination reduces die size while performing
both voice processing and system control.

DEPR:
FIG. 1 shows the organizational relationship of the major components of the
communications processor 100 of the present invention. CPU 200 may be a
convention 80186 type processor such as the model 80C186 microprocessor sold by
Advanced Mirco Devices of Sunnyvale Calif. This processor includes a clock
generator 202, a bus interface 204, an execution unit 206, a direct memory
access unit 208, a chip select unit 210, timers 212, and an interrupt processor
214. In accordance with the present invention, CPU 200 can be programmed by a
user to implement user designated functions and operates in conjunction with
**DSP** 300 to carry out VSELP in accordance with IS-54 and other signal processing
algorithms, as will be explained in greater detail below.

DEPR:
CPU 200 communicates with SRAM 400 and **DSP** 300 through a bus system which
includes address bus 102 and data bus 104. These busses also provide
communication to a transmit/receive buffer 500 and an audio interface section
600.

DEPR:
As will be understood by reference to FIG. 1, communications to a base station
or the like, if a **cellular** phone system implementation is adopted, is made
through buffer 500 which can connect to a transmission system including a
modem, a **radio** or the like. Communication to the local user is made through
interface 600 which connects to a microphone and a speaker, as will be

discussed in greater detail below.

DEPR:
On the receive side, the 16 kHz output of the **speech processor** is interpolated in hardware unit 612 and fed into D/A converter 606. The output of the D/A feeds either the earpiece, loudspeaker, or both. A programmable analog gain stage is located in each path (0.fwdarw.-36 dB; 3 dB steps). The earpiece driver can drive a 540 Ohm load at 5V P-P. The loudspeaker driver can drive a 40 Ohm load at 5V P-P. With 0 dB of gain programmed into either path, a full-scale digital code produces the full-scale output voltage.

DEPR:
The Multiply/Accumulate (MAC) engine 300 is a special purpose **DSP** engine designed to work with the CPU 200 to perform complex speech processing algorithms. The MAC engine is shown in greater detail in FIG. 4 to include an execution unit 302, a sequencer 304, various loop counters 306, 308 and address generators 310, 312, an instruction ROM 314, and an external interface to the SRAM 400. The MAC may also include conventional **DSP** features such as a 24 bit.times.24 bit hardware multiplier and hardware do loops to help carry out its specialized function.

DEPR:
As mentioned above, the CPU operates both as the system CPU and as part of the **speech processor**. What the user actually sees is a portion of the CPU processing capacity. The partitioning between system functions and speech processing is enforced by the OS support logic block, and a firmware shell. The scheduling mechanism is static in nature, giving the CPU resource to the speech operation unconditionally at very specific times. When the CPU is not

performing speech related tasks, it is available for system functions. As a consequence of the static scheduling, the user sees the CPU for a portion of the time, with rigidly enforced gaps when the processor is unavailable. These gaps are transparent to the user, with the exception that the CPU is not working on non-speech tasks during the gaps. This means that all system tasks including interrupts are blocked (held off) during speech processing windows.

DEPR:
GSM--In GSM mode, the following functions are performed on the Speech channel: In the receive direction, the HDLC (LAPM) bit level processing is handled in the control channel processor, and the data is placed in the internal SRAM. In the transmit direction, packets are formatted by the 80C186 and placed into the internal SRAM. From there, the control channel **processor executes the bit level HDLC protocol** and passes the data to the frame formatter.

DEPR:
FIG. 20 shows the telephone functions for analog operating mode. In this mode, the communications **processor performs the all of the required speech** and control functions. It is interesting to note that communications **processor 100 processes the speech** and control signals using the same **DSP** resources used for the digital mode. The A/D and D/A converters present in the digital mode DQPSK modem are used in the analog mode to convert the analog signal present at the radio to and from a digital format. This reduces the duplication of hardware that would otherwise be required for dual-mode operation.

DEPR:
FIG. 19 is a time graph divided into four time lines of 5 ms each. Points or lines above the main time line indicate operation of the

CPU and points or
lines below the main time line indicate operation of the **DSP** of MAC engine.
Cross hatching indicates simultaneous operation of the CPU and **DSP**. The
operations are partitioned here so that multiply or multiply and accumulate
operations are performed by the **DSP**, which is adapted for such calculations due
to its hardware multipliers, hardware do loops, etc. Other operations, such as
additions, subtractions, divides, square roots, exclusive ORs, look-up tables
and compares are performed by the CPU. The execution of these partitioned
operations is scheduled to take advantage of as much simultaneous operation of
the CPU and **DSP** as is feasible in order to reduce the total time required to
execute the entire procedure. It will be understood by reference to the
figures that this means some of the calculations are performed before they are
actually required.

DEPR:
The approach chosen takes advantage of the high bandwidth A/D and D/A resources
required in the digital modem (digital voice operation) to convert the analog
mode signal into digital form. Once the analog signals have been digitized,
the **DSP** resources required in digital mode can be used to process the speech
(emphasis/deemphasis, compression/expansion, etc.) and control (SAT, FSK modem,
etc). The major open architectural decision remaining is the partitioning of
these tasks between the **DSP** engine in the MSC and the **DSP** engine in the digital
modem. While the MSC has the horsepower to perform the required functions,
using the digital modem's **DSP** reduces the data rate required between the
communication processor 100 and the digital modem--this is important since this
serial channel is carried in the cable between the handset and the radio box in

applications where the radio is not built into the handset.

DETL:
TABLE 1 Function Encoder E No. of Arithmetic Operations Frame/Subframe No
Decoder D **DSP** CPU F/SF Comments E 1 High Pass Filter 1440 F 160 samples E 2
Autocorrelation & Windowing 1870 + 55 F E 3 Covariance Lattice Algorithm 1475
10 F E 4 Convert r.sub.i to .alpha..sub.i 45 SF E 5 Interpolate .alpha..sub.i
20* SF *subframes 1, 2, 3 only E 6 Reconvert to r.sub.i - stability 90* 9 SF
*subframes 1, 2, 3 only E 7 Calculate Long-term Predictor Lag 11556 126 SF E
8 Zero-state Response of each codevector to H(Z) 2450 F Codebook 1 search E
9 Interpolate zero-state response 280* SF *subframes 1, 2, 3 only E 10
Orthogonalise codevectors 600 1 SF E 11 Calculate Rm, Dmj 280 + 1120 SF E 12
Calculate Ci, Gi, Cu, Gu 616 SF E 13 Calculate Ci.sup.2 G.sub.best &
C.sub.best.sup.2 Gi 192 SF E 14 Compare values 64 SF End of codebook 1
search E 8' as 8 for codebook 2 2450 F Codebook 2 search E 9' as 9 for
codebook 2 280 SF *subframes 1, 2, 3 only E 10'
Orthogonalise codebooks 1 and
2 6320 8 SF E 11' as 11 for codebook 2 280 + 1120 SF E 12' as 12 for codebook
2 616 SF E 13' as 13 for codebook 2 192 SF E 14' as 14 for codebook 2 64 SF
End of codebook 2 search E 15 Calculate Rec, Rx(i) 240 + 40 SF Gain
Quantisation E 16 Calculate RS, Rpc 22 + 120 SF E 17 Calculate
a,b,c,d,e,f,g,h,i 21 3 SF E 18 E 19 Gain error minimisation 2304 SF E 20
Compare gain error values 255 SF E 21 Calculate .beta..sub.q .gamma..sub.1q
.gamma..sub.2q 3 SF E 22 Generate selected codevectors 560 SF E 23 Generate
combined excitation 120 SF E 24 Update weighted synthesis Filter 400 SF E 25
Update long-term Filter states SF Address pointer update D 1 Convert r.sub.i
to .alpha..sub.i 45 SF D 2 Autocorrelate Postfilter 55 +

55 + 10 F Subframe 4
only, item impulse resp. interpolate D 3 Binomial
Windowing of Autocorr. 10
F D 4 Levinson Recursion (.eta.) 110 10 F D 5 Interpolate
.alpha..sub.i 20*
SF *subframes 1, 2, 3 only D 6 Convert to r.sub.i -
stability 90* 9 SF
*subframes 1, 2, 3 only D 7 Calculate Rq(o) Frame energy
SF D 8 Interpolate
Frame energy 1 SF D 9 Calculate RS 22 SF D 10 Transform
GS,PO,Pq to Pq
.gamma..sub.1q .gamma..sub.2q 40 + 9 3 SF D 11 Generate
combined excitation
120 560 SF D 12 Update synthesis filter A(Z) 400 SF D 13
Update long-term
filter states SF Address pointer update D 14 Update
spectral post filter 840
SF D 15 Signal scaling 122 2 SF

CLPR:
2. An apparatus as claimed in claim 1 wherein said **digital signal processing**
algorithm is a digital speech processing algorithm and said
scheduling means is
contained in said **dsp**.

CLPR:
3. An apparatus as claimed in claim 2 wherein said
scheduling means causes all
multiply/multiply and accumulate operations to be processed
in said **dsp** and all
other operations to be processed in said cpu.

CLPR:
9. An apparatus as claimed in claim 1 wherein said
scheduling means effects
simultaneous operation of said cpu and **dsp** during portions
of the execution of
said signal processing algorithm.

CLPR:
13. An apparatus as recited in claim 12 further comprising
a shared memory
accessible by said **dsp** and said cpu via separate paths.

CLPR:
14. An apparatus as recited in claim 13 wherein said cpu
performs

predetermined portions of the signal processing algorithm upon request by said **dsp**.

CLPV:
wherein said **dsp** executes signal processing operations and wherein said cpu executes a first and second group of tasks, said first group of tasks performing non signal processing operations independent of said **dsp** and said second group of tasks being a subset of said signal processing operations, said second group of tasks having a higher priority than said first group of tasks, said cpu executing said second group of tasks in response to receipt on said non-maskable interrupt input of an interrupt generated by said **dsp**.

CLPW:
a **digital signal processor (dsp) having a dsp** instruction set to carry out a **digital signal processing** algorithm, an execution unit for carrying out multiply and accumulate operations and an external interface, said **dsp** being capable of executing simultaneously with said cpu;

CLPW:
an address bus connected between said cpu and said **dsp**;

CLPW:
a memory accessible by said cpu and said **dsp**;

CLPW:
a scheduling means for statically scheduling execution of one algorithm between said cpu and said **dsp**, said scheduling means transmitting non-maskable interrupts to said cpu non-maskable interrupt input to effect execution of portions of said algorithm to be executed by said cpu; and

CLPW:
a data bus connected between said cpu and said **dsp**.

CLPW:
a **digital signal processor (dsp) having a dsp** instruction set to carry out a
**digital signal processing** algorithm, an execution unit for carrying out
multiply and accumulate operations and an external interface, said **dsp**
executing simultaneously with said cpu;

CLPW:
scheduling means for statically scheduling execution of the signal processing
algorithm between said **digital signal processor** and said cpu;

CLPW:
wherein said cpu instruction set and said **dsp** instruction set have minimum
overlapping instructions.

CLPW:
a **digital signal processor (dsp) having a dsp** instruction set to carry out a
**digital signal processing** algorithm, an execution unit for carrying out
multiply and accumulate operations and an external interface, said **dsp**
executing simultaneously with said cpu;

CLPW:
an address bus connected between said cpu and said **dsp**;

CLPW:
a multi-port memory independently accessible by said cpu and said **dsp**;

CLPW:
a data bus connected between said cpu and said **dsp**; and

CLPW:
said **dsp** including scheduling means for statically scheduling execution of the
signal processing algorithm between said **digital signal processor** and said cpu
and transmitting interrupt signals to said cpu non-maskable interrupt input;
and